REMARKS

Applicants respectfully requests reconsideration of this application as amended. No claims have been amended, added, or cancelled. Therefore, claims 1-31 are present for examination.

The amendments to the claims made by this Response are not being made for the purpose of patentably distinguishing the claimed invention over the prior art. Instead, the amendments within are solely for the purpose of spelling out an abbreviated term. None of the amendments made by this Response add new subject matter, and all of the amendments made by this Response are fully supported by the originally filed application.

35 U.S.C. §102(b) Rejection

Leger et al.

Claims 1-31 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Leger et al. (hereinafter Leger, U.S. Patent No. 5,771,356) in view of Garcia et al., (hereinafter Garcia, U.S. Patent No. 6,493,343).

Leger discloses a data management mechanism for a FIFO (first-in-first-out) buffer that allows a system bus to be used more efficiently. Data transfer by the FIFO buffer is controlled by acquiring the system bus based on the amount of data in the FIFO buffer and on the state of the system bus. Leger maintains a soft threshold and a hard threshold, and monitors the FIFO buffer to determine if

the FIFO buffer has crossed the thresholds. The system bus can be casually acquired when the FIFO buffer reaches the soft threshold and the system bus is idle. The system bus can be aggressively acquired when the FIFO buffer reaches the hard threshold. The thresholds are dynamically adjustable. Additionally, casual and aggressive control can be relinquished under certain conditions, including the amount of data transferred. (See Leger, for example, Abstract, column 2, lines 39-67.)

Garcia discloses a system and method for facilitating in-order and out-of-order packet reception in a SAN (system area network).

Applicants respectfully submit that the combination of Leger and Garcia does not make obvious claims 1-31 of the subject application. At the least, neither Leger nor Garcia discloses "associating portions of the second buffer region with a second transfer operation if the determining determines that the size of the first buffer region exceeds the maximum transfer" as required by each of claims 1-31. The Examiner cites various portions of Leger to support a contrary position. For example, the Examiner refers to FIG. 4A; Abstract; column 2, line 6 - column 3, line 13; column 9, lines 15-30; and column 9, line 47 – column 10 line 11. However, none of these cited portions of Leger discloses this claim element.

For example, in Leger, if "xfer_cnt 713 is equal to or greater than curr_xfr_cnt signal 716 indicating that the requested data transfer is complete, comparator 709 generates a high signal to OR gate 714 which in turn generates

stopXFR signal 720 to relinquish control of system bus 204" (Leger, column 9, lines 27-31). Applicants do not find where any of these cited portions disclose, teach, or suggest "associating portions of the second buffer region with a second transfer operation if the determining determines that the size of the first buffer region exceeds the maximum transfer". Instead, Leger clearly discloses that when the number of bytes left in the buffer exceeds the threshold value, control of the system bus is relinquished.

Since the combination of Leger and Garcia does not disclose, teach, or suggest each and every element of claims 1-31, Applicants respectfully submit that claims 1-31 are patentable over the combination of Leger and Garcia. Consequently, Applicants respectfully request that the Examiner withdraw the rejections to claims 1-31, and allow the claims as amended.

Conclusion

Applicants respectfully submit that the claims as amended are in condition for allowance. Therefore, allowance at an early date is earnestly solicited.

The Examiner is invited to initiate an interview with the undersigned by calling 949-498-0601 if the Examiner believes that such an interview will advance prosecution of this application.